34. (Currently Amended) A method of manufacturing a semiconductor component comprising:

providing a substrate having a surface;

forming by a non LOCal Oxidation of Silicon (LOCOS) process, a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region in the substrate;

forming a channel region in the substrate, at least a portion of the drift region located between the channel region and the non-electrically conductive region; and

forming an electrically floating region in the substrate and contiguous with the non-electrically conductive region;

wherein at least a portion of the electrically floating region is located between the non-electrically conductive region and the channel region, at least a portion of the electrically floating region is located laterally with respect to the non-electrically conductive region, and at least a portion of the electrically floating region is located underneath the non-electrically conductive region.

35. (Original) The method of claim 34 wherein forming the channel region and forming the electrically floating region occur simultaneously with each other.

36. (Previously Presented) The method of claim 34 wherein the forming by a non LOCal Oxidation of Silicon (LOCOS) process, the non-electrically conductive region further comprises:

etching a trench into the surface of the substrate; and

filling the trench with a material.

37. (Previously Presented) The method of claim 36 wherein the material includes a semi insulative material.

38. (Previously Presented) The method of claim 36 wherein the material includes a dielectric material.

39. (Previously Presented) The method of claim 36 wherein the material includes at least one of silicon dioxide, silicon nitride, and gallium arsenide.

40. (Previously Presented) The method of claim 36 further comprising:
forming a thermal liner oxide layer along walls of the trench prior to the filling.

41. (Previously Presented) The method of claim 36 further comprising:
densifying the material.

42. (Previously Presented) The method of claim 36 further comprising:
planarizing the material.

43. (Previously Presented) The method of claim 34 wherein the forming by a non LOCal Oxidation of Silicon (LOCOS) process, the non-electrically conductive region further includes implanting a dose of oxygen into the surface at a substrate at location corresponding to non-electrically conductive region.

44. (Previously Presented) A method of manufacturing a semiconductor component comprising:
providing a substrate having a surface;
forming by a non LOCal Oxidation of Silicon (LOCOS) process, a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;
forming a drift region in the substrate;
forming a channel region in the substrate, at least a portion of the drift region located between the channel region and the non-electrically conductive region; and
forming an electrically floating region in the substrate and contiguous with the non-electrically conductive region;
wherein at least a portion of the channel region, at least a portion of the non-electrically conductive region, at least a portion of the drift region, and at least a portion of the electrically floating region are located at the surface of the substrate.

45. (Previously Presented) The method of claim 34 wherein at least a portion of the electrically floating region is located between the drift region and the non-electrically conductive region.

46. (Previously Presented) The method of claim 45 wherein at least a portion of the channel region, at least a portion of the non-electrically conductive region, at least a portion of the drift

region, and at least a portion of the electrically floating region are located at the surface of the substrate.

47. (Previously Presented) The method of claim 46 wherein a portion of the electrically floating region at the surface of the substrate is located between a portion of the drift region at the surface of the substrate and a portion of the non-electrically conductive region at the surface of the substrate.

48. (Previously Presented) The method of claim 56 wherein the electrically floating region is located between the drift region and the non-electrically conductive region.

49. (Previously Presented) The method of claim 56 wherein at least a portion of the electrically floating region is located underneath the non-electrically conductive region.

50. (Previously Presented) The method of claim 56 wherein the electrically floating region is located only underneath the non-electrically conductive region.

51. (Previously Presented) A method of manufacturing a semiconductor component comprising:

providing a substrate having a surface;

forming by a non LOCal Oxidation of Silicon (LOCOS) process, a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region in the substrate;

forming a channel region in the substrate, at least a portion of the drift region located between the channel region and the non-electrically conductive region; and

forming an electrically floating region in the substrate and contiguous with the non-electrically conductive region;

forming a drain region in the substrate;

wherein:

the non-electrically conductive region is located between the drain region and the channel region; and

at least a portion of the electrically floating region is located between the non-electrically conductive region and the drain region.

52. (Previously Presented) The method of claim 51 wherein at least a portion of the channel region, at least a portion of the non-electrically conductive region, at least a portion of the drift region, and at least a portion of the electrically floating region are located at the surface of the substrate.

53. (Previously Presented) The method of claim 56 wherein at least a portion of the electrically floating region is located between the non-electrically conductive region and the channel region and at least a portion of the electrically floating region is located underneath the non-electrically conductive region.

54. (Previously Presented) The method of claim 34 wherein at least a portion of the channel region, at least a portion of the non-electrically conductive region, at least a portion of the drift region, and at least a portion of the electrically floating region are located at the surface of the substrate.

55. (Previously Presented) The method of claim 34 wherein the channel region is electrically isolated from a portion of the substrate located underneath the channel region.

56. (Currently Amended) A method of manufacturing a semiconductor component comprising:

providing a substrate having a surface;

forming by a non LOCal Oxidation of Silicon (LOCOS) process, a non-electrically conductive region substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region in the substrate;

forming a channel region in the substrate, at least a portion of the drift region located between the channel region and the non-electrically conductive region; and

forming an electrically floating region in the substrate and contiguous with the non-electrically conductive region;

wherein the channel region is electrically coupled to a portion of the substrate located underneath the channel region;

wherein at least a portion of the channel region, at least a portion of the non-electrically conductive region, at least a portion of the drift region, and at least a portion of the electrically floating region are located at the surface of the substrate.

57. (Previously Presented) The method of claim 34 further comprising:

forming a gate electrode over the surface of the substrate,

wherein:

the channel region is located under the gate electrode;

the drift region is located at least partially under the gate electrode; and

the electrically floating region is located at least partially under the gate electrode.

58. (Previously Presented) The method of claim 57 wherein:

the electrically floating region has a doping type;

the drift region has an other doping type different from the doping type of the electrically floating region and is located under the electrically floating region, and

a portion of the substrate has the doping type of the electrically floating region and is located under the drift region and under the electrically floating region.

59. (Previously Presented) The method of claim 58 wherein the electrically floating region is located under the non-electrically conductive region.

60. (Previously Presented) The method of claim 58 wherein the non-electrically conductive region is located under the gate electrode.

61. (Previously Presented) The method of claim 34 wherein:

the electrically floating region has a doping type;

the drift region has an other doping type different from the doping type of the electrically floating region and is located at least partially under the electrically floating region, and

a portion of the substrate has the doping type of the electrically floating region and is located at least partially under the drift region and located at least partially under the electrically floating region.

62. (Previously Presented) The method of claim 44 wherein:

the electrically floating region comprises a first portion and a second portion;

the first portion of the electrically floating region is located at least partially underneath the non-electrically conductive region; and

the second portion of the electrically floating region includes a portion that is located at the surface of the substrate between a portion of the drift region at the surface of

the substrate and a portion of the non-electrically conductive region at the surface of the substrate.

63. (Previously Presented) The method of claim 62 wherein the first portion of the electrically floating region is separate from the second portion of the electrically floating region.

64. (Previously Presented) The method of claim 34 further comprising:
forming a gate dielectric over at least a portion of the non-electrically conductive region.

65-69. (Canceled)

70. (New) The method of claim 34 wherein at least a portion of the electrically floating region is located laterally between the non-electrically conductive region and the channel region.